



Recorder Integrated Processor and Router



“RIPR”



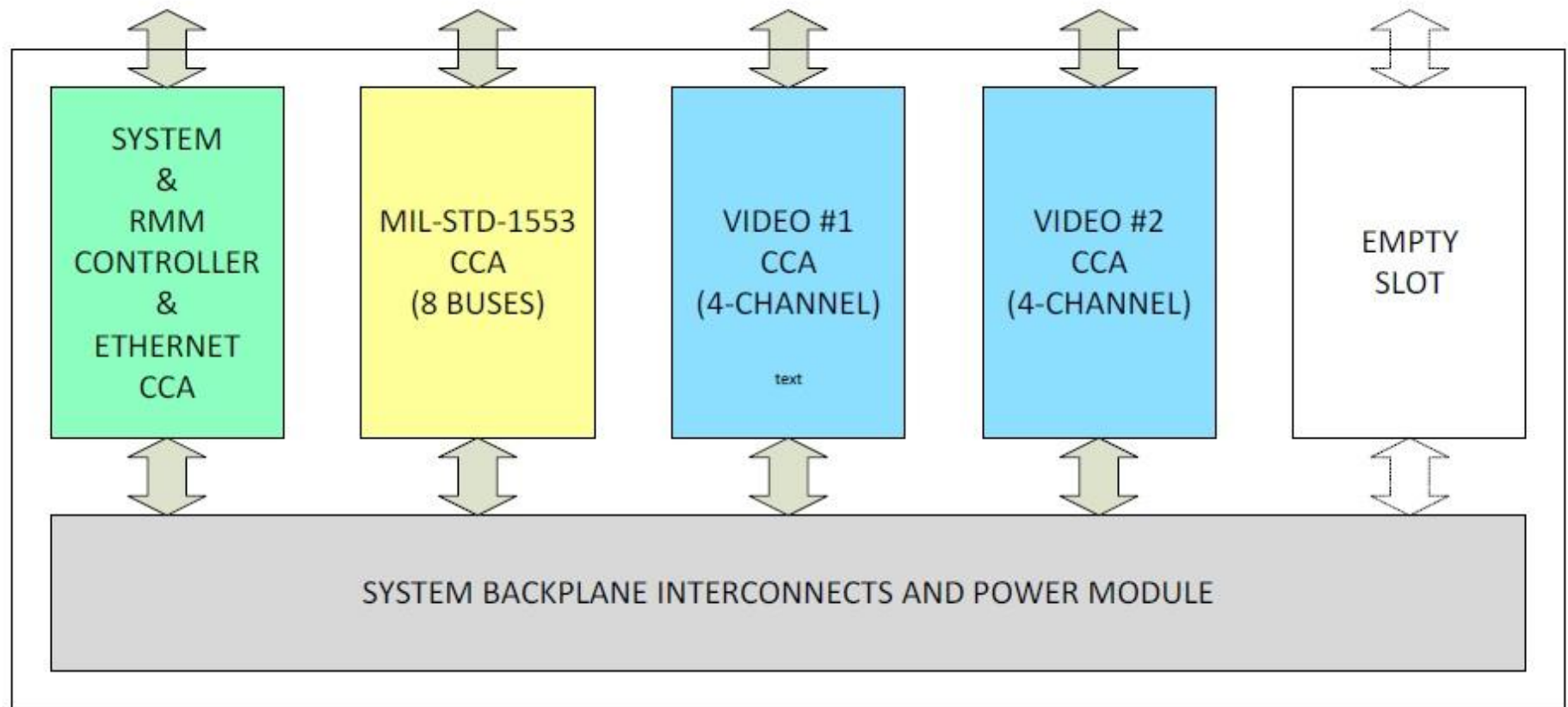


Background

- Conceived by Major Jerry “Stoner” Reedy, F-15 Action Officer
- and
- Major Todd “Malibu” Giggy, Director F-15 OPS
- Joint Venture – Lockheed Martin Missiles and Fire Control
- First Successful Flight – 88 Days From Conception To Flight at Jacksonville IAP
- Objective: Provide F-15C/D Fleet SNIPER Pod Night Vision and Tracking



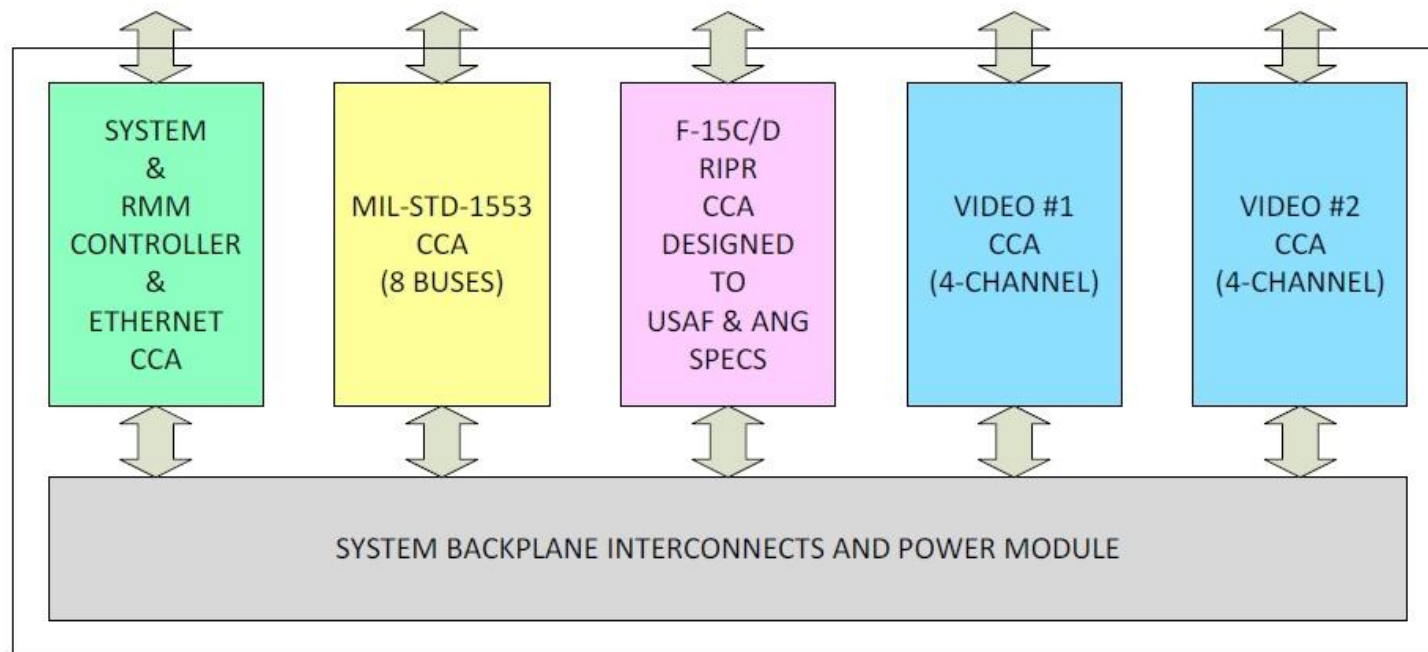
What Made The Project Work?



F-15 DVR & FDR



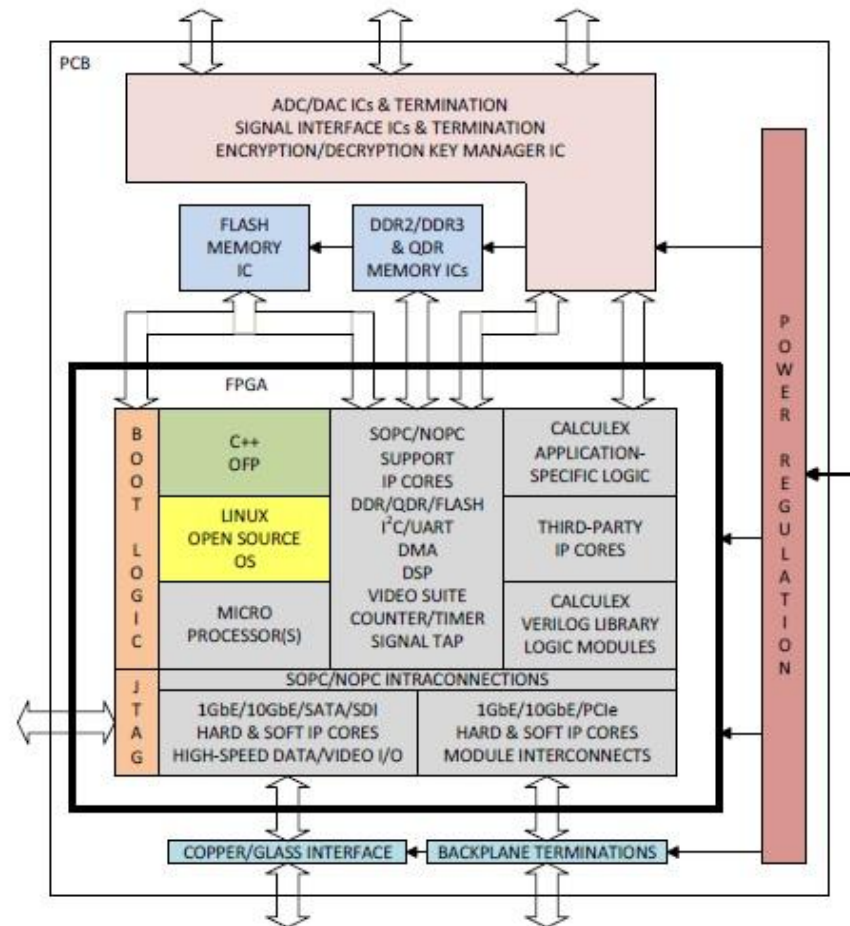
Add Processor Board



F-15 RIPR

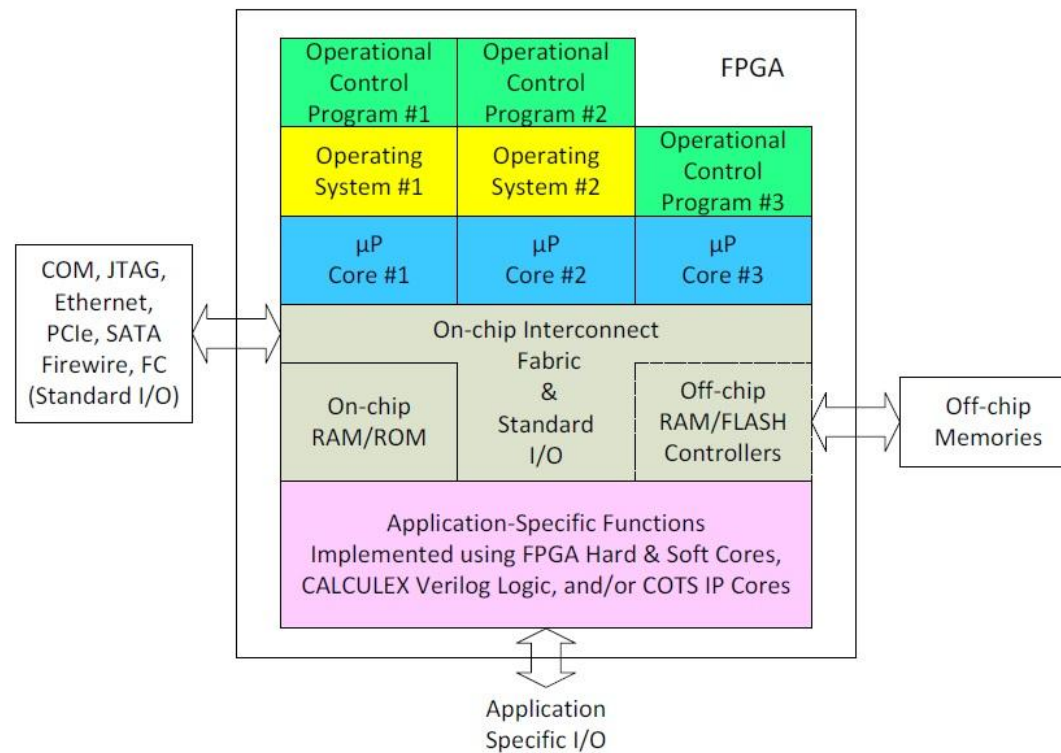


CALCULEX “Soft” Architecture





Field Programmable Gate Array





Start With DVR





Add DAU and CSMU





Add Processor Board



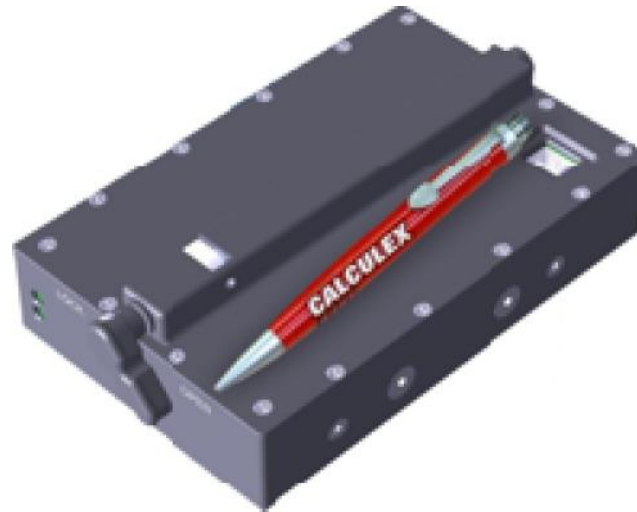


CSR-2300(V2) Recorder





Removable Memory Module (RMM)





Flight Data Recorder (FDR)





F-15C/D and E Basic Features

- Six video + audio input channels with
 - Programmable input per channel (composite, S-Video, monochrome) with NTSC or PAL format
 - Programmable frame rate (30 or 25) per channel
 - Programmable absolute system day/time overlay position and resolution per channel
 - Programmable time overlay foreground/background mode (black on white or clear, white on black or clear)
 - Separate stereo audio CODEC per video channel supports single local input and global audio resampling for perfect video/audio synchronization
 - Separately programmable L and R stereo audio source per channel, either local or resampled global audio



F-15C/D and E Basic Features

- Six MIL-STD-1553 Bus Monitor (MT) channels with
 - Dual programmable message filters per channel for separate classified and unclassified recordings (files)
 - Programmable word selector per channel for retriggerable one-shot and/or repetitive capture of selected bus words passed to controller module for RT responses or system control functions
- Eight RS-422 pairs configured as 8-in, 4-in/4-out, or 8-out
 - Can support synchronous, asynchronous, and custom protocols for data recording, data output, and/or control functions
 - Optional bit-sync logic enables clock extraction from data-only inputs



F-15C/D and E Basic Features

- Power supply mechanical and electrical design criteria extends life
 - Circuit design uses multiple COTS MIL-spec modules
 - Normal operation at 50%-60% rated capacity minimizes thermal stresses on components for extended life
 - Power supply base plate is system chassis bottom plate for optimum conduction cooling
- Eight input and eight output opto-coupled discretes
 - Inputs can be strapped for active high (aircraft +28VDC) or active low (chassis GND) operation
 - Outputs can include optional series current limiting resistors
- Meets MIL-STD-704F 50ms power loss coverage



Conclusion

- CALCULEX designs are flexible, extensible and powerful
- The RIPR project started with a sketch and discussion by two pilots that wanted the Air National Guard and Air Combat Command F-15C/D aircraft to have SNIPER pod tracking and night vision
- “What’s new is that we have developed a valid, plug-and-play, open architecture, integration model that may be repeatable for other (sensor and electronic warfare) systems.”, Major Giggy pointed out
- **The genesis for the ease-of-upgrade is the variable capabilities required to support the test and evaluation community**



Questions

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